ANALOG DEVICES

AN-636
APPLICATION NOTE

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ADN2819 Evaluation Board

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INTRODUCTION

This application note describes the use of the ADN2819 evaluation board. The ADN2819 is a multirate clock recovery, data-retiming device based on a multiloop PLL architecture. The ADN2819 can recover clock and data at SONET OC-3, OC-12, OC-48, and Gigabit Ethernet data rates as well as 15/14 Forward Error Correction (FEC) for these rates by using a single reference clock or external crystal oscillator.

The ADN2819 evaluation board is fabricated using standard FR-4 materials. All high speed signal traces are matched to within 1 mil length and maintain a 50 Ω characteristic impedance to preserve signal integrity. The ADN2819 evaluation board is also used for the ADN2811.

QUICK START GUIDE FOR OC-48, NORMAL OPERATING MODE

1. Apply a 3.3 V supply to the AVCC and GND vector pins.
2. Connect PIN/NIN to a pattern generator that can supply a differential input of greater than 10 mV to the ADN2819. Use cables of matching length.
3. Connect CLKOUTP/N, DATAOUTP/N to measurement equipment using cables of matching length.
4. All switches S1 through S9 should be in the 0 position.* This sets the part up in OC-48, normal operating mode, using the on-board 19.44 MHz crystal as the reference clock.
5. Apply a single-ended or differential 2.488 Gbps NRZ data stream to the ADN2819 inputs. The recovered 2.488 GHz clock and retimed data will be present at the CLKOUTP/N and DATAOUTP/N outputs, respectively.

*For a 0, the red switch should be in the right-most position as shown in Figure 1. For ADN2819 evaluation boards that are populated with 3-pin jumpers instead of the slide switches, the jumper should be placed on the left-most two pins for a 0.

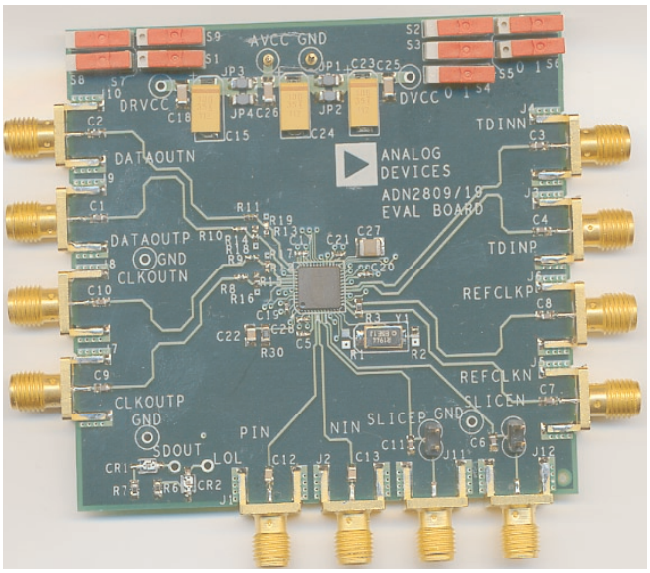

Figure 1. ADN2819 Evaluation Board (Actual Size)

POWER SUPPLY

The ADN2819 evaluation board requires a single 3.3 V nominal supply for basic operation. This supply is brought on board through vector pins AVCC and GND at the top center of the board. The evaluation board is shipped configured for a single supply through jumpers JP1 through JP4, which are populated with ferrite beads. If these ferrite beads are removed, separate 3.3 V supplies must be applied to the vector pins labeled DVCC and DRVCC. This allows the user to keep the analog supply, digital supply, and output driver supply separate, though it is not required.

DATA RATE SELECTION

The input data rate of the ADN2819 is selected by SEL0, SEL1, SEL2 switches S2 through S4 (see Table I). The ADN2819 can be programmed to acquire OC-3 (155.52 Mbps), OC-3 FEC (166.6 Mbps), OC-12 (622.08 Mbps), OC-12 FEC (666.5 Mbps), OC-48 (2.488 Gbps), OC-48 FEC (2.665 Gbps), Gigabit Ethernet (1.25 Gbps), and Gigabit Ethernet FEC (1.339 Gbps).

Table I. Data Rate Selection

SEL2	SEL1	SEL0	Rate	Frequency
0	0	0	OC-48	2.48832 GHz
0	0	1	GbE	1.25 GHz
0	1	0	OC-12	622 MHz
0	1	1	OC-3	155.5 MHz
1	0	0	OC-48 × 15/14	2.666 GHz
1	0	1	GbE × 15/14	1.339 GHz
1	1	0	OC-12 × 15/14	666.5 MHz
1	1	1	OC-3 × 15/14	166.6 MHz

REFERENCE CLOCK

The ADN2819 has an on-chip crystal oscillator that is used with a 19.44 MHz external crystal resonator in series resonant mode. When the REFSEL pin is set to 0, the crystal oscillator is used to supply the reference frequency. If an external clock oscillator or other external reference clock is used, the REFSEL pin is set to 1 and an external reference clock is brought in either differentially or single-ended on the REFCLKP/N pins.When configured to use an external reference clock, the ADN2819 XTAL oscillator is disabled by populating R1 and R2 with 1 kΩ pull-up resistors.

The ADN2819 can accept any of the following reference clock frequencies: 19.44 MHz, 38.88 MHz, or 77.76 MHz at LVTTL/LVCMOS/LVPECL/LVDS levels or 155.52 MHz at LVPECL/LVDS levels via the REFCLKN/P inputs. The reference clock frequency is selected independent of data rate. Only a single reference clock rate needs to be selected for the ADN2819 to operate over all data rates. Setting REFSEL switch S1 to (1) disconnects the on-board 19.44 MHz crystal oscillator and selects the external reference clock inputs, REFCLKN/P on SMA connectors J5 and J6. REFCLKN/P accepts any differential signal with a peak-to-peak differential voltage level of greater than 100 mV (e.g., LVPECL or LVDS), or a single-ended LVTTL or LVCMOS input.

The REFCLK inputs are high impedance. However, on the evaluation board there is a 100 Ω resistor, R3, placed across REFCLKP and REFCLKN to provide a differential 100 Ω termination in case the REFCLK inputs are being driven by a 100 Ω differential source impedance. If this 100 Ω termination is not required, (e.g., the reference clock is being driven single-ended by a clock oscillator), R3 should be removed. The external reference clock frequency is selected by REFSEL0, REFSEL1 switches S5 through S6 (see Table II).

Table II. Reference Frequency Selection

REFSEL1	REFSEL0	Applied Reference Frequency (MHz)
0	0	19.44
0	1	38.88
1	0	77.76
1	1	155.52

LOOP FILTER CAPACITOR

The loop filter capacitor, C_F, is connected between the CF1 and CF2 pins 21, 25. The recommended capacitor parameters are shown in Table III. The ADN2819 evaluation board uses a low leakage 4.7 μF X7R capacitor.

Table III. Recommended Capacitor Specifications

Parameter	Value
Capacitance (–40°C to +85°C)	4.7 μF
Leakage (–40°C to +85°C)	< 80 nA
Rating	6.3 V

PIN/NIN INPUTS

PIN/NIN inputs are brought onto the ADN2819 evaluation board through SMA connectors J1 and J2. Capacitors C3, C4 provide ac coupling to the on-chip 50 Ω termination resistors. When ac coupling the inputs and outputs of the ADN2819, care must be taken when choosing ac coupling capacitor values. The time constant formed with the 50 Ω resistors in the signal path must be considered. Also, when a large number of consecutive identical digits (CIDs) are applied, the capacitor voltage can droop, causing pattern dependent jitter. The designers of the ADN2819 have done a thorough investigation at the OC-3 and OC-48 data rates, and have come to the following conclusion. Assuming that 1000 CIDs must be tolerated, a minimum capacitor of 1.6 μF to PIN/NIN, and 0.1 μF on DATAOUTP/DATAOUTN should be used. The ADN2819 evaluation board is shipped with 1.8 μF X7R capacitors in the C1, C2 positions to optimize performance at the OC-3 data rate.

CLOCK/DATA OUTPUTS

CLKOUTP and CLKOUTN are brought out through 0.1 μF ac coupling capacitors to SMA connectors J7 and J8, respectively. DATAOUTP and DATAOUTN are brought out through 0.1 μF ac coupling capacitors to SMA connectors J9 and J10, respectively.

SLICEP/SLICEN

SLICE allows the ADN2819's input quantizer decision level to be adjusted to accommodate amplified spontaneous emission (ASE) in fiber amplifier applications. The slicing level can be adjusted by up to ± 100 mV by applying a differential input voltage of up to ± 800 mV to SLICEP/SLICEN. The SLICEP and SLICEN inputs are brought onto the ADN2819 evaluation board through SMA connectors J11 and J12, respectively. When not being used, the SLICEN/SLICEP inputs should be tied to VCC using the jumpers.

LOL (LOSS OF LOCK)

The ADN2819 lock detector monitors the frequency difference between the VCO and the reference clock. The loss of lock (LOL) signal is deasserted when the VCO is within 500 ppm of the center frequency. If the frequency error between the input data rate and the selected data rate then

drifts to more than 0.1% (1000 ppm), the LOL output will be asserted. LED CR2 provides a visual indication of LOL status; it will turn on when the part has lost lock.

The LOL output is LVTTL compatible and shows the lock status of the frequency detector loop. Loss of lock output is brought out to a test point labeled LOL.

SDOUT (SIGNAL DETECT OUTPUT)

SDOUT/LOS uses peak detection circuitry to determine if the input data to the quantizer is above the threshold set by THRADJ resistor R30. The SDOUT output is LVTTL compatible. LED CR1 provides a visual indication of SDOUT status; it turns on when a loss of signal condition is detected. SDOUT is also brought out to a test point labeled SDOUT.

SQUELCH

When the SQUELCH input, Pin 39, is driven to a TTL high, both the clock and data outputs are set to the zero state. Switch S7 is provided to drive the SQUELCH pin high or low. If the SQUELCH function is not required, the SQUELCH pin should be driven low.

TEST MODES

Test Data Inputs, TDINN/TDINP

The test data inputs, TDINN and TDINP, facilitate the use of an external quantizer/limiting amplifier bypassing the ADN2819's input quantizer to provide direct input to the clock recovery circuit. Test data inputs TDINN and TDINP are brought onto the ADN2819 evaluation board through SMA connectors J3 and J4, respectively.

Test modes are enabled using LOOPEN, Pin 48, and BYPASS, Pin 44. These are LVTTL/CMOS compatible logic inputs. Switches S8 and S9 are used to set BYPASS and LOOPEN, respectively.

Table IV shows how to set all the test modes.

BYPASS Mode

Asserting the BYPASS input through the BYPASS switch S8 connects the output of the quantizer directly to the data output buffers, bypassing the clock recovery circuit. This affects only the data output circuitry. The clock output remains connected to the clock recovery circuit and continues to output a valid clock if the input data rate is valid.

LOOPEN Mode

Asserting the loop enable input through the LOOPEN switch S9 connects the test data inputs TDINN and TDINP through the input multiplexer to the clock recovery circuit. This function can be used for testing the clock recovery functionality as well as for configuring the ADN2819 for use with an external limiting amplifier/quantizer.

Table IV. ADN2819 Test Modes

LOOPEN	BYPASS	Function
0	0	Normal Operation
0	1	BYPASS Mode
1	0	LOOPEN Mode

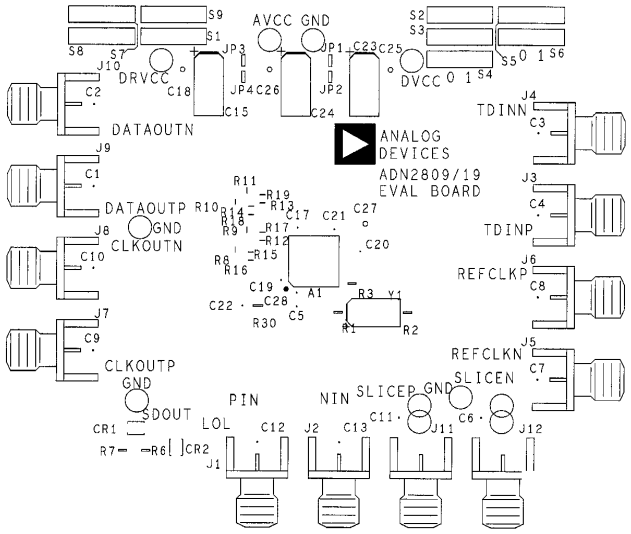

Figure 2. Silkscreen Layer

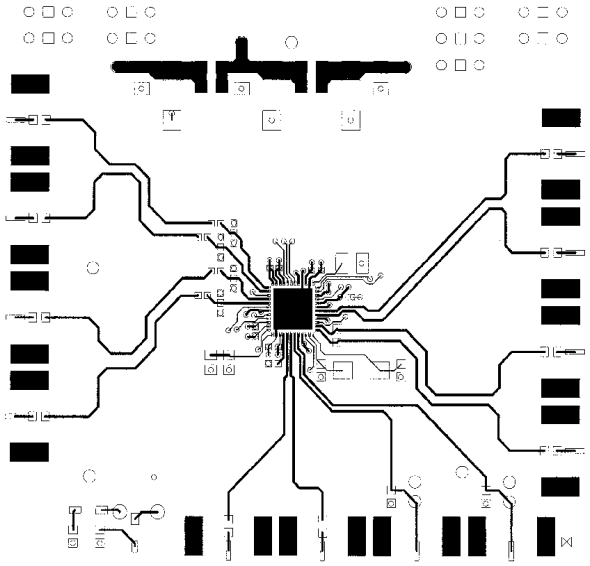

Figure 3. Top Layer

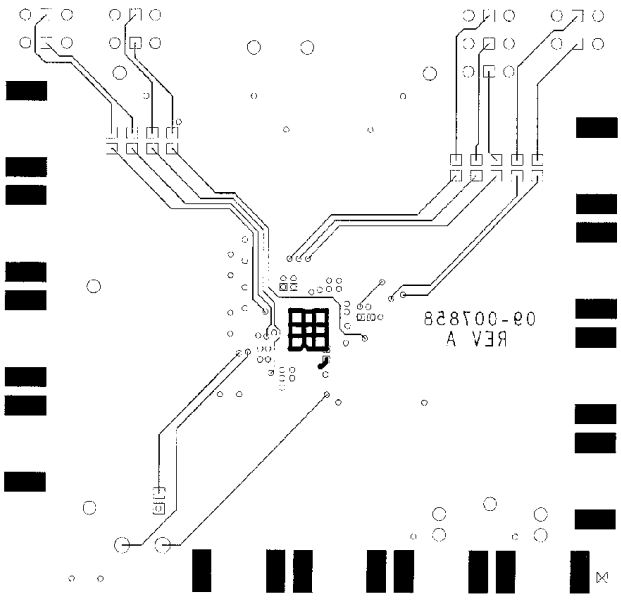

Figure 4. Bottom Layer

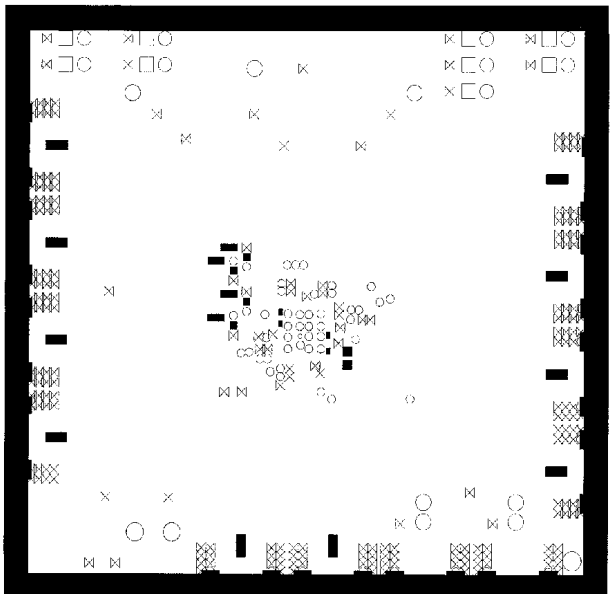

Figure 5. Ground Plane

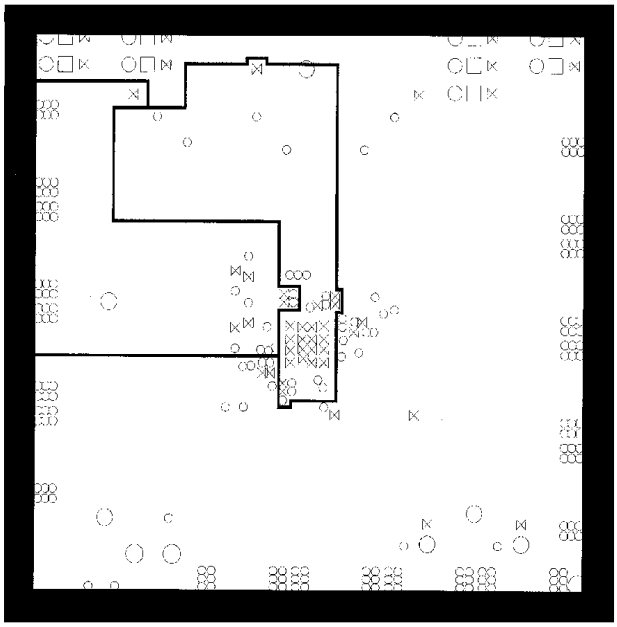

Figure 6. Power Plane

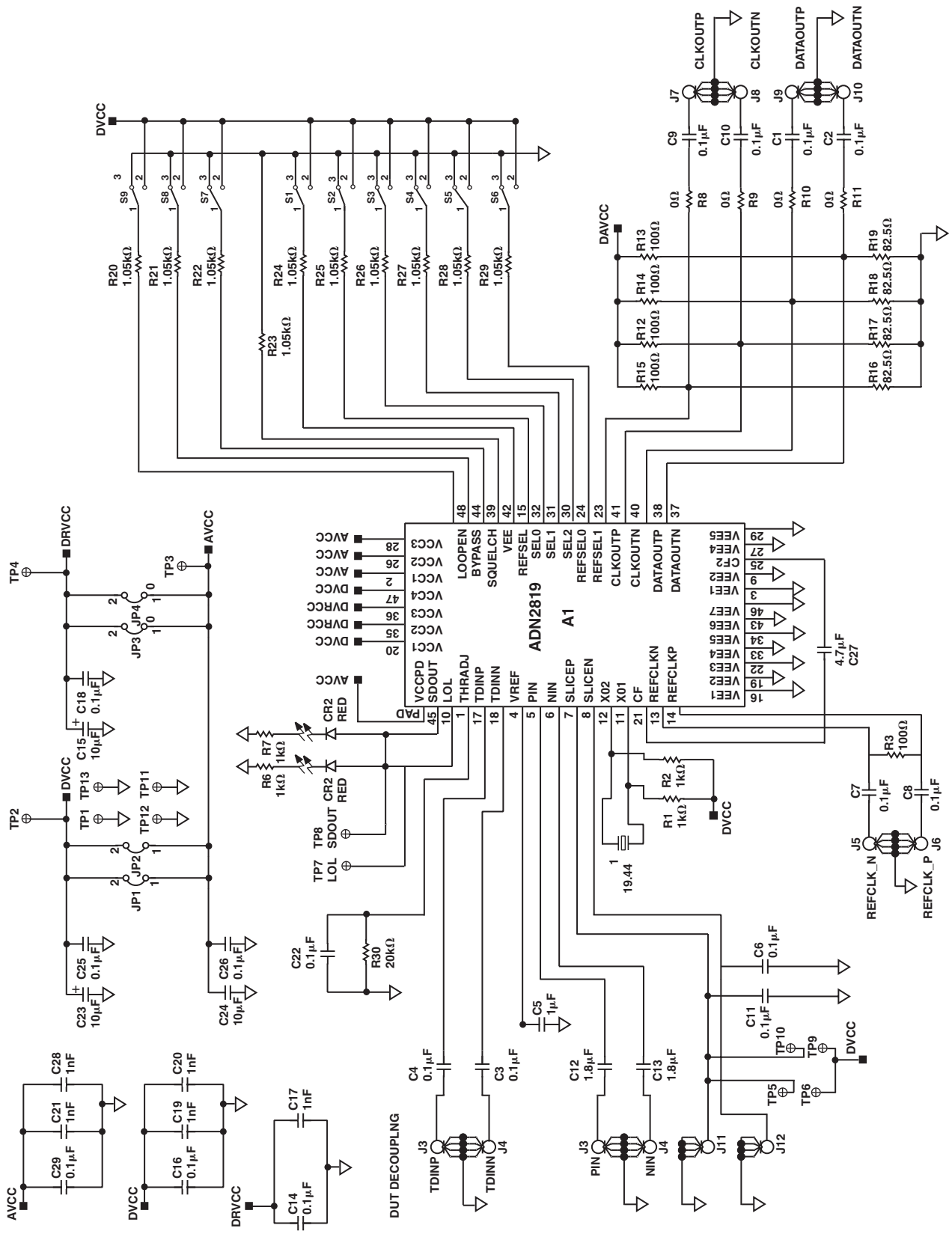

Figure 7. Evaluation Board Schematic

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